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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Title: INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD

Docket No.: 1303.024US2

Serial No.: 10/789,038

Filed: February 27, 2004

Due Date: N/A

Examiner: Ly D. Pham

Group Art Unit: 2811

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
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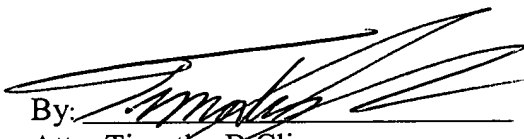
We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ A Communication Concerning Related Applications (2 pgs.).
- ☒ A Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.). Documents NOT enclosed.

Please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

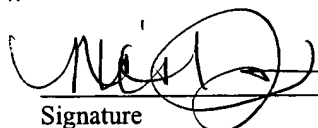
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

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By:   
Atty: Timothy B Clise  
Reg. No. 40,957

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Name

  
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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
(GENERAL)



S/N 10/789,038

PATENT

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COMMUNICATION CONCERNING RELATED APPLICATIONS

Commissioner for Patents  
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Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related applications in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/945,395 6,754,108	August 30, 2001	1303.019US1	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/943,134	August 30, 2001	1303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945,498 6,778,441	August 30, 2001	1303.024US1	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD
09/945,512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945,554	August 30, 2001	1303.028US1	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/081,818	February 20, 2002	1303.045US1	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS
10/177,096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER



INTERPOLY INSULATORS

10/783,695	February 20, 2004	1303.019US2	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/781,035	February 18, 2004	1303.063US2	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/788,810	February 27, 2004	1303.027US2	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/819,550	April 7, 2004	1303.019US3	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

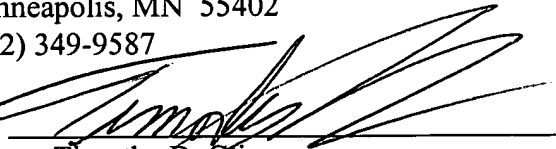
Respectfully submitted,

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Date 17 Aug '04

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